Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

Claims 1-18 (canceled).

19. (currently amended) An optical disk drive apparatus, comprising:

an optical disk drive mechanism; and

an interface circuit for interfacing communications between the optical disk drive mechanism and a host computer, the interfacing circuit comprising:

an input terminal for receiving data sent from the host computer;

a data processor configured to perform a predetermined data processing operation to the data received through the input terminal;

a clock generator configured to generate a clock signal with which the data processor performs the predetermined data processing operation;

an operation mode changer configured to control the clock generator to reduce a frequency of the clock signal to a non-zero value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode;

a buffering circuit block configured to buffer the data received through the input terminal of the optical disk drive apparatus from the host computer, the buffering circuit block including:

a first data transfer path configured to transfer the data received through the input terminal to the data processor not via a memory, and

a second data transfer path configured to transfer the data received through the input

terminal to the data processor via a memory; and

a path selection controller configured to control the buffering circuit block to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode.

20. (previously presented) The optical disk drive apparatus of claim 19, wherein the path selection controller selects one of the first and second data transfer paths for a write operation.

Claim 21 (canceled).

22. (currently amended) An optical disk drive apparatus, comprising:

an optical disk drive mechanism configured to read data from an optical disk medium;

a register circuit including a plurality of registers configured to store data read by said optical disk drive mechanism from said optical disk medium and to be transferred from the optical disk drive apparatus to a host computer;

a first memory configured to store first information indicating specific addresses of corresponding specified registers in the register circuit and representing an access executed by the host computer to the optical disk drive mechanism for a data transfer;

a second memory configured to store second information, [[sent]] received by said second memory in association with the first information stored in the first memory and corresponding to said data read by said optical disk drive mechanism from said optical disk medium and to be transferred from the optical disk drive apparatus to said host computer, to be

written into the specified registers at the specific addresses indicated by the first information stored in the first memory; and

a control circuit configured to perform an information writing operation for writing the first information and the second information into the first memory and ~~the second information into~~ the second memory, respectively, in chronological order of accesses executed, in connection with said data read by said optical disk drive mechanism from said optical disk medium and to be transferred from the optical disk drive apparatus to said host computer.

23. (previously presented) The optical disk drive apparatus according to Claim 22, wherein the control circuit performs the information writing operation to write the first information into the first memory and the second information into the second memory in the chronological order of the accesses executed, when an operation mode of the optical disk drive apparatus is changed from a low power consumption mode to a regular operation mode.

24. (previously presented) The optical disk drive apparatus according to Claim 22, wherein the control circuit performs an information reading operation for reading the first and second information written in the first and second memories, respectively, in the chronological order of the accesses executed and an information transfer operation to transfer the first and second information read from the first and second memories, respectively, to the register circuit in the chronological order of the accesses executed, when an operation mode of the optical disk drive apparatus is changed from a low power consumption mode to a regular operation mode.

25. (previously presented) The optical disk drive apparatus according to Claim 22,

wherein each of the first and second memories comprises a first-in and first-out memory including a specific number of buffer areas into which data from the host computer is written, and the control circuit conducts information writing operations with respect to the first and second memories in synchronism with each other and conducts information reading operations with respect to the first and second memories in synchronism with each other.

26. (previously presented) The optical disk drive apparatus according to Claim 25, wherein the control circuit transfers the first and second information directly to the register circuit, without buffering the first and second information in the first-in and first-out memories of the first and second memories, in an event that the respective first-in and first-out memories of the first and second memories are in a memory empty state after the first and second information stored in the respective first-in and first-out memories of the first and second memories, respectively, are transferred to the register circuit when an operation mode of the optical disk drive apparatus is changed from a low power consumption mode to a regular operation mode.

27. (previously presented) The optical disk drive apparatus according to Claim 25, wherein each of the first and second memories comprises a selection circuit configured to select one of (i) a first data path for the first and second information not via the first and second memories and (ii) a second data path for the first and second information via the respective first and second memories, on an exclusive basis according to a control signal from the control circuit and to output corresponding data to the register circuit through the selected one of the first and second data paths.

28. (previously presented) The optical disk drive apparatus according to Claim 27, wherein the control circuit comprises:

a data writing circuit block configured to write the first and second information into the first and second memories, respectively, in accordance with an access performed by the host computer;

a data reading circuit block configured to start reading the first and second information from the first and second memories, respectively, upon a time the data writing circuit block starts writing the first and second information into the first and second memories, respectively;

a status detecting circuit block configured to detect memory statuses of the first-in and first-out memories included in the respective first and second memories and to output a status signal representing the memory statuses detected; and

a selection control circuit block configured to control the selection circuits included in the respective first and second memories in accordance with a status as to whether an operation mode of the optical disk drive apparatus is a low power consumption mode and the status signal output from the status detecting circuit block.

29. (previously presented) The optical disk drive apparatus according to Claim 22, wherein the control circuit accesses the first and second memories in synchronism with a first clock signal for the information writing operation and a second clock signal for an information reading operation, and wherein a first frequency of the first clock signal is greater than a second frequency of the second clock signal.

30. (previously presented) The optical disk drive apparatus according to Claim 22,

wherein the register circuit, the first and second memories, and the control circuit are integrated into a single integrated chip.

31. (currently amended) A method for transferring data between an optical disk drive apparatus and a host computer, said method comprising the steps of:

reading data by an optical disk drive mechanism of the optical disk drive apparatus from an optical disk medium;

storing in a register circuit of the optical disk drive apparatus data read by said optical disk drive mechanism from said optical disk medium and to be transferred to a host computer;

storing in a first memory of the optical disk drive apparatus first information indicating specific addresses of corresponding specified registers in the register circuit and representing an access executed by the host computer to the optical disk drive apparatus for a data transfer, and storing in a second memory of the optical disk drive apparatus second information, [[sent]] received by said second memory in association with the first information stored in the first memory and corresponding to said data read by said optical disk drive mechanism from said optical disk medium and to be transferred from the optical disk drive apparatus to said host computer, to be written into the specified registers of the register circuit at the specific addresses indicated by the first information stored in the first memory; and

performing an information writing operation with a control circuit for writing the first information and the second information into the first memory and ~~the second information into~~ the second memory, respectively, in chronological order of accesses executed, in connection with said data read by said optical disk drive mechanism from said optical disk medium and to be transferred to said host computer.

32. (previously presented) The method of claim 31, wherein the information writing operation to write the first information and second information into the first memory and second memory, respectively, is performed when an operation mode of the optical disk drive apparatus is changed from a low power consumption mode to a regular operation mode.

33. (previously presented) The method of claim 31, further comprising the steps of:

executing an information reading operation for reading the first and second information written in the first and second memories, respectively, in the chronological order of the accesses; and

conducting an information transfer operation for transferring the first and second information read from the first and second memories, respectively, to the register circuit in the chronological order of the accesses executed, when an operation mode of the optical disk drive apparatus is changed from a low power consumption mode to a regular operation mode.

34. (previously presented) The method of claim 34, wherein a first clock signal is utilized for synchronizing the information writing operation and a second clock signal is utilized for synchronizing the information reading operation, and a first frequency of the first clock signal is greater than a second frequency of the second clock signal.

35. (previously presented) The method of claim 31, wherein each of the first and second memories includes a first-in and first-out memory including a specific number of buffer areas into which data from the host computer is written, and information writing operations are

performed to write the first information and second information into the first and second memories, respectively, in synchronism with each other and information reading operations are performed with respect to the first and second memories in synchronism with each other.

36. (previously presented) The method of claim 35, wherein the first and second information are transferred directly to the register circuit without buffering the first and second information into the first-in and first-out memories of the first and second memories, in an event that the respective first-in and first-out memories of the first and second memories are in a memory empty state after the first and second information written in the respective first-in and first-out memories of the first and second memories, respectively, are transferred to the register circuit when an operation mode of the optical disk drive apparatus is changed from a low power consumption mode to a regular operation mode.

37. (previously presented) The method of claim 35, further comprising the steps of:

generating a selection control signal;

selecting one of (i) a first data path not via the first and second memories and (ii) a second data path via the respective first and second memories, on an exclusive basis according to the selection control signal; and

outputting corresponding data to the register circuit through one of the first and second data paths selected.

38. (previously presented) The method of claim 37, further comprising:

instructing the information writing operation to write the first and second information

into the first and second memories, respectively, in accordance with an access performed by the host computer;

instructing an information reading operation to start reading the first and second information from the first and second memories, respectively, upon a time the information writing operation starts writing the first and second information into the first and second memories, respectively;

detecting memory statuses of the first-in and first-out memories included in the respective first and second memories; and

controlling the selection of one of (i) and (ii) in accordance with the memory statuses detected and a status as to whether an operation mode of the optical disk drive apparatus is a low power consumption mode.

39. (new) The optical disk drive apparatus of claim 19, wherein in said regular operation mode, a first clock signal of a first frequency of said predetermined value is supplied from the clock generator to the data processor, and in said low power consumption mode, a second clock signal of a second frequency of said non-zero value is supplied from the clock generator to the data processor.

40. (new) The optical disk drive apparatus of claim 19, wherein the clock generator includes a clock generation circuit configured to generate concurrently a plurality of clock signals of respective non-zero frequencies, and one of said plurality of clock signals of respective non-zero frequencies is selected to be output as said clock signal of said clock generator.